Plan for DAQ at SuperKEKB/Belle

R. Itoh, KEK

1. Possible DAQ condition in SuperKEKB/Belle
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4. Upgrade scenario
1. Possible DAQ condition in SuperKEKB/Belle

- Target Luminosity : $3\sim5 \times 10^{35}/\text{cm}^2/\text{sec}$
- Detector
  Tracker : Silicon(+Pixel) + Drift Chamber
  Calorimetry : CsI(Tl) (Barrel) + Pure CsI(End Cap)
  PID : TOP (Barrel) + Aerogel RICH (End Cap)
  $\mu/K^{-}$ detection : RPC(Barrel) + Scintillation Tile(End Cap)
Detector Electronics Quick Summary

- SVD : CMS APV25 chip
- Pixel : MAPS(CAP3) or “striplet” = short sillicon strip
- CDC : 3 approaches
  1) Pipelined TDC with Q-to-T conversion (shorter shaping time)
  2) ADC with waveform sampling (10bit@>200MHz)
     (or TDC + FADC (TMC+12bitFADC@20MHz) )
- ECL : Wave form sampling needed to manage pileup effect
  (12bit FADC@2MHz for barrel, >20MHz for pure CsI)
- TOP/RICH : Need to manage pixel photo-detector
  * Time stretcher, HPTDC, Analog pipeline
- KLM : Readout scheme is not so much different from Belle's
  regardless of choice of detection device (RPC/Sci. Tile)
  * "hit" info multiplexing + on-board data compression
## Expected event size at L1

<table>
<thead>
<tr>
<th></th>
<th>Belle</th>
<th>SuperKEKB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel(Striplet)</td>
<td>-</td>
<td>~100KB(30KB)</td>
</tr>
<tr>
<td>SVD</td>
<td>15KB</td>
<td>~30KB</td>
</tr>
<tr>
<td>CDC</td>
<td>6KB</td>
<td>~10KB(-&gt;100KB)</td>
</tr>
<tr>
<td>PID</td>
<td>3KB(TOF/ACC)</td>
<td>~20KB</td>
</tr>
<tr>
<td>ECL</td>
<td>8KB</td>
<td>~100KB</td>
</tr>
<tr>
<td>KLM</td>
<td>3KB</td>
<td>~3KB</td>
</tr>
<tr>
<td>TRG/others</td>
<td>3KB</td>
<td>~3KB</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>~40KB</td>
<td>~300KB</td>
</tr>
</tbody>
</table>

* CDC: wave form sampling might be necessary for higher occ.
* ECL: wave form sampling is necessary for pileup effect (~10 buckets/hit*12bit)
  => can be reduced to 1/5 by feature extraction

* Overall event size compression using word-packing/"zip"
  -> 100KB/ev before event builder
L1 trigger

- Keep Belle's trigger scheme
- Trigger latency 2.2us (Belle) >5 us
- More intelligent trigger is being considered
L1 Rate @ SKEKB : Rough Estimation

<table>
<thead>
<tr>
<th>Exp.</th>
<th>Rate</th>
<th>Luminosity</th>
<th>Current</th>
<th>Magic Number</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Rate / Lum</td>
<td>Rate @ 10^35</td>
<td>Rate / Current</td>
</tr>
<tr>
<td>7</td>
<td>200</td>
<td>13</td>
<td>13 k</td>
<td>210</td>
</tr>
<tr>
<td>17</td>
<td>250</td>
<td>4.5</td>
<td>4.5 k</td>
<td>130</td>
</tr>
<tr>
<td>27</td>
<td>350</td>
<td>4.4</td>
<td>4.4 k</td>
<td>150</td>
</tr>
</tbody>
</table>

- Vacuum is the biggest factor to estimate the rate
- CDC Z-trigger is included in above numbers
  - We have to live @ SKEKB without Z triggers
    - ~30% increase without Z trigger (Exp.31)
      4.4 kHz x 1.3 = 5.7 kHz
    - On the other hand, if we have SVD Z-trigger, we can reduce L1 rate by factor 2~5.
- Very important
  - We can not know real BG situation in SKEKB

Physics Rate 1.0 k
## Estimated DAQ condition at SuperKEKB

<table>
<thead>
<tr>
<th></th>
<th>Belle</th>
<th>SuperKEKB ($L=\sim3\times10^{35}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physics trigger rate</td>
<td>100 Hz</td>
<td>3 KHz</td>
</tr>
<tr>
<td>Maximum trigger rate</td>
<td>500 Hz</td>
<td>10~30 KHz</td>
</tr>
<tr>
<td>Event size at L1</td>
<td>40KB/ev</td>
<td>200~300KB/ev</td>
</tr>
<tr>
<td>Data flow rate at L1</td>
<td>20MB/s</td>
<td>&gt;2 GB/sec</td>
</tr>
<tr>
<td>Data flow at storage</td>
<td>10MB/s</td>
<td>&lt;250MB/sec</td>
</tr>
<tr>
<td>Subdetector readout</td>
<td>26</td>
<td>&gt;1000</td>
</tr>
<tr>
<td>HLT reduction</td>
<td>2</td>
<td>&gt;10</td>
</tr>
</tbody>
</table>
2. DAQ Design for Super KEKB

Input: ~ 100K channels

~1000 Pipeline ROM(COPPER) (pipelined readout)

~50 Readout PCs

~10 Event Building Farms

~10 L3 Farms

Transfer Network

mass storage

Current DAQ

all components are Linux-based PC's
- 9U VME board
- Most of the functions are provided by add-on modules
  * Digitizers (FINESSE) / CPU (PMC CPU Card)
**Timing Distribution**

- **2-step cascade** from GDL
- **High-speed serial bus on LVDS**

- Master TT-IO module
- 1-8 TT-Switch (TT-SW) switches
- 64 distribution by 2-step cascade (4096 by 4-step)
- TT-Receiver (TT-RX) on each COPPER
Multi-stage event building

* Event Building is done in 3 steps.
  Stage 1: Collect event fragments from CoPPERs in a crate
  Stage 2: Collect event fragments from one subdetector
  Stage 3: Build complete one event

* Common event building software framework at all stages
  ("switchless event builder" + BASF)

Stage 1 Event Building

- CoPPER
  - ~20 boards/crate
  - x ~50 crates
- 100BaseTX SW
- 100baseTX
- 1000BaseT
- Readout PC
Stage 2 event building

* Collect event fragments from 1 subdetector at event builder input
Stage 3 event building

* Full event building

* Keep current scheme at Belle: switchless event building farm

- Level 2.5 trigger software on E1 node
- Event rejection at E2 node
Level 3 Trigger Farm/Storage

* Full event reconstruction capability is necessary to achieve ultimate data reduction.
* A PC cluster is connected to event builder output.

1 Unit → processing power for $L=2 \times 10^{34}/cm^2/sec$  ~20 Units for design $L$
3. R&D status

Common Readout Platform: COPPER

Form factor = VME 9U

- $O(100)$ of the COPPER boards are used by each sub-detector system.
- Total $O(1000)$ COPPER boards.

**FINESSE modules**

COPPER module by KEK.
TDC FINESSE with AMT-3

- Block diagram of TDC FINESSE sequence controller

TDC FINESSE module by KEK elec. group.
Flash ADC FINESSE

- 8 ch differential input
- Sampling clock = 65 MHz
- Dynamic range = 12 bit
- Linearity = 1.2%
- Equips 512 word/ch FIFO

(500 MHz FADC FINESSE of 2 ch / 8 bit has also been developed)

The FINESSE with higher channel density is under design.
Timing Distribution

**Receiver module (TT-RX)**
- PMC standard
- Attach onto the TT-RX slot of COPPER
- Flexible logics on Spartan-3 (Test Triggers, FIFO, error detection, monitoring, LVDS I/O)
- Finalized after iterations (version 4)
  - version 3 uses Spartan-2 and has an inconvenient cable assignment

**Distribution switch (TT-SW)**
- Standard VME 6U module
- All information on a single Spartan-3 (XC3S400) FPGA (distribution, handshake, monitoring)
Performance test of Stage 2 Event Building

Setup in KEK
6x6 network matrix

We measured network performance of SenderPCs.
Performance study - stage 2

The prototype setup can endure high rate by increasing the number of Receiver PCs.

The graph shows the total transfer rate (MB/s) against event size (byte) for different numbers of receiver PCs. At typical data size, the scalability increases with the number of receiver PCs. The equation for scalability is:

\[ \text{Scalability} = \frac{\text{EventRate (receiver } = 2 \sim 6\)}{\text{EventRate (receiver } = 1\)} \]
L3 Trigger Farm / Storage

E-hut

Belle Event
Builder

DTF

Computer Center

Server room

Dell
CX600

input
distributor

Dual Xeon(3.0GHz)

output
collector

Dual Xeon(2.8GHz)

Planex
FMG-226SX

disk server

DNS

NIS

control

Dual PIII(1.3GHz)

3com
4400

Dual Athlon
1.6GHz

3com
4400

85 nodes
(170 CPUs)

PCs are operated by Linux (RH7.3)

- 1000base/SX
- 100base-TX

85 nodes

....

input
distributor

100base-TX
Athlon Servers
(3 racks are used for RFARM)
### 4. Upgrade Scenario

**Possible DAQ condition until SuperB upgrade**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Trigger Rate</th>
<th>Deadtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>L ~ $1.5 \times 10^{34}$ in 2004-2005</td>
<td>$500-700$ Hz</td>
<td>3-4%</td>
</tr>
<tr>
<td>L ~ $2-3 \times 10^{34}$ in 2005-20xx (with crab cavity installed)</td>
<td>$1-2$ kHz</td>
<td>10%</td>
</tr>
<tr>
<td>L &gt; $10^{35}$ in 20xx (xx can be 08~11?) by SuperB upgrade</td>
<td>$10$ kHz (max. 30 kHz)</td>
<td></td>
</tr>
</tbody>
</table>

(Belle's DAQ is not pipelined)

- Needs effort to reduce deadtime and to increase processing power for event builder/L3 farm

- Pipelined DAQ is really necessary for increased CPU power for EB/L3 farm
“Smooth” step-by-step upgrade strategy

Goal: keep < 5% intrinsic DAQ deadtime at any time

* Replace existing FASTBUS TDC system with COPER based pipelined TDC system detector by detector during scheduled accelerator shutdown time (Summer, Winter)
  - Start from the detector with the longest readout deadtime (CDC) next FY.
  - Repeat replacement whenever deadtime becomes serious until Super-B upgrade

* Modularize backend DAQ (event builder+reconstruction farm) and add new units whenever more processing power is required.
Upgrade of Digitizers

Replace FASTBUS TDC system to COPPER based TDC system

Event Builder

FastEther

Trigger (SEQ)

Readout PC

Network SW

COPPER

VME 9U

TT-SW

Controller

FPI

TDM

Gate Generator

LeCroy 1877S

FASTBUS

LeCroy 1877S

LeCroy 1877S

FastEther

GbE

X n

Trigger
Upgrade of Event Builder/RFARM

Current DAQ: Readout subsystems are connected to single Event Builder through point-to-point network connection

- Modularize (Event Builder + RFARM) as a unit
- Have multiple units
## Upgrade Timeline

<table>
<thead>
<tr>
<th>Fiscal Year</th>
<th>Description</th>
</tr>
</thead>
</table>
| FY2004      | - Complete R&D on COPPER  -> Almost done  
              - TDC FINESSE design and production -> in progress |
| FY2005      | **Summer**  
              - Replacement of EFC TDCs with COPPER TDCs  
              - 2\textsuperscript{nd} unit of Event Builder + RFARM  
              **Winter (during crab cavity installation period)**  
              - Replacement of CDC |
| FY2006      | - New timing distribution system  
              - Replacement of KLM and TRG |
| FY2007      | - Replacement of TOF and ACC  
              - 3\textsuperscript{rd} unit of Event Builder+RFARM (if necessary) |
| FY2008      | - Full upgrade of Readout for ECL Barrel part (wave form smpl.)  
              - SVD readout upgrade(?) / SVD upgrade? |
| FY2009      | - Full upgrade of Readout for ECL Endcap part |
| FY20xx      | - Full upgrade with new electronics / new FINESSE  
              - Operation with 10 units of Event Builder+RFARM |

*Super B*